Instruction:

**Name:Noil Chitrakar Group:L4CG1**

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?
2. Program and Data stored in Separate Memory
3. Program and Data stored in the same Memory
4. Program and data stored in Cache Memory
5. All of the Above
6. Which of the following is the working cycle of the CPU?
7. Decode, Execute, Fetch
8. Fetch, Decode, Execute
9. Fetch, Execute, Decode
10. All of the Above
11. Any condition that causes a processor to stall is called \_\_\_\_\_\_\_\_\_
12. Hazard
13. Page fault
14. System error
15. None of the mentioned
16. What does the control unit generate to control other units?
    1. Transfer signals
    2. Command Signal
    3. Control signals
    4. Timing signals
17. What must the processors of all computers have?
    1. Control unit
    2. ALU
    3. Register
    4. All of these
18. Which is the fastest memory in the computer?
19. Cache
20. RAM
21. Register
22. Hard disk
23. With the help of \_\_\_\_\_\_\_, we reduce the memory access time:
    1. SDRAM
    2. Cache
    3. Heaps
    4. Higher capacity RAMs
24. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
    1. ISA
    2. ANSA
    3. Super-scalar
    4. All of the mentioned
25. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_
    1. Super-scaling
    2. Pipe-lining
    3. Parallel Computation
    4. None of the mentioned
26. A 24 bit address generates an address space of \_\_\_\_\_\_ locations.
    1. 1024
    2. 4096
    3. 248
    4. 16,777,216
27. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

Ans: Given: The country size for 1st row: 40\*8 =320bit

The name size for 1st row: 2\*8=16bit

The population for 1st row: 32bit

The median for 1st row:32bit  
 The total of all the 1st row and 1st column:400 bit

The total of all the 3100 counties:400\*3100= 1240000bit

Converting the bit into bytes: (1240000/8)=155000 bytes

Converting the bytes to kilobytes: (155000/1024)=151.37 kilobytes.

Therefor, the whole database would take in 151.37 kilobytes in memory

1. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
2. Calculate the width of the data bus.

TM=DB\*AS  
2^37=DB\*2^32  
therefor:DB=2^5

1. State the effect that adding one new line to the address bus would have on the maximum addressable memory.

ANS:

Total memory= ?

The origina, address bsu=2^32

The new Address bus=2^33 as one new line is added

Data bus=2^5

Now,

Total original memory= Data bus\*Address bus =2^5\*2^32 =16GB

Total new memory= Data bus\*Address bus =2^5\*2^33 =32GB

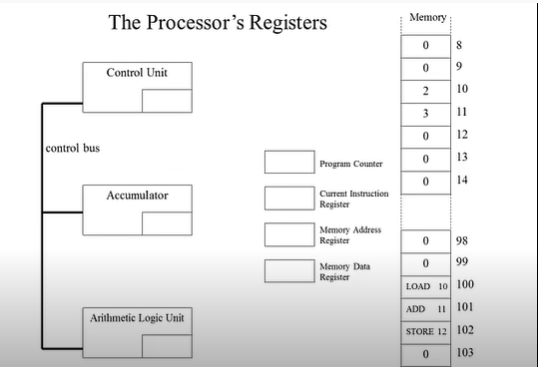
This 32 GB is double Than 16GB hence ,  
the memory doubles when one new line is added to the address bus.

1. Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add : [11]

Store: [12]



ANS:the instruction cycle is as follows:

First,

1. The memory address of the instruction is copied from the program counter into the memory address register.
2. The instruction is then fetched from the main memory and placed in the memory address register.
3. The instruction in the memory address register is transferred to the current instruction register.
4. The instruction is decoded by the control unit and executed.
5. The program counter is incremented by one to point to the next instruction.
6. If the current instruction requires data to be fetched from the memory (e.g. instruction ADD 11), the main memory address of the data is copied into the memory address register and the data is transferred from the main memory to the memory data register and then to the ALU.
7. If the current instruction requires data in the accumulator register to be saved in the main memory (e.g. instruction STORE 12), the memory address is copied into the memory address register, the data is transferred from the accumulator to the memory data register, and then to the main memory.

1. Write short notes on the following topic:
2. Von Neumann and Harvard Architecture

ANS:

Von Neumann

1) Von Neumann architecture stored data and instruction in the same memory  
2)Two clock cycles are required to execute single instruction.

3)CPU can not access instructions and read/write at the same time.

4)it is cheap

5)It is used in personal computers and small computers.

Harvard Chitecture

1)Harvard Architecture had separate buses and memory for data and instruction

2)An instruction is executed in a single cycle.

3) CPU can access instructions and read/write at the same time.

4) IT is expensive than Von Neumann architecture

5) It is used in micro controllers and signal processing.

1. RISC vs CISC architecture

ANS:

RISC

1. A Reduced Instruction Set Computer (RISC) is a type of computer architecture that uses simple, standardized instructions that can be executed quickly.
2. RISC processors rely heavily on software to program them, and they are known for their single-cycle instructions, which allow them to execute instructions quickly.
3. RISC processors make heavy use of RAM, which can cause bottlenecks if the amount of available RAM is limited.
4. Examples of RISC architectures include ARM, Alpha, and AVR.

CISC  
1) A Complex Instruction Set Computer (CISC) is a type of computer architecture that uses complex and variable length instructions that can take several clock cycles to execute.

2) CISC processors emphasize hardware optimization of the instruction set, and they are known for their ability to more efficiently use RAM than RISC processors.

3) Some examples of CISC architectures include VAX, AMD, and the Intel x86 CPUs.